AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application.

Claims 1-54 (Cancelled)

55. (Currently Amended) A system comprising:

a connector to a bus;

an instruction memory to store a plurality of bus stimuli instructions that represent a predefined sequence of bus transactions, [[wherein]] each transaction [[has]] including a plurality of transaction phases; and

[[one or more phase generators]] a phase generator coupled [[between]] with the instruction memory and the connector, the [[one or more]] phase generator [[generators]] to receive the plurality of bus stimuli instructions from the instruction memory and to provide a plurality of signals [[on]] to the bus [[that represent the predefined sequence of bus transactions]] based on the instructions.

56. (Currently Amended) The system of claim 55, wherein the predefined sequence of bus transactions comprises a user specified sequence of bus transactions [[that has been specified by a user in]] based on a high level language.

57. (Previously Presented) The system of claim 55, wherein the predefined sequence of bus transactions comprises an illegal sequence of bus transactions.

58. (Previously Presented) The system of claim 55, wherein the predefined sequence of bus transactions is based on an existing simulation stimulus software.

59. (Currently Amended) The system of claim 55, wherein the predefined sequence of bus transactions is [[the same as a corresponding predefined sequence of bus transactions specified in an existing]] based on a simulation stimulus software.

60. (Currently Amended) The system of claim 55, wherein an instruction of the plurality of bus stimuli instructions comprises an instruction word having a predefined length, the instruction word containing a plurality of predefined segments, each of the plurality of segments to provide instruction to a different portion of the [[one or more]] phase generator [[generators]].

61. (Currently Amended) The system of claim 55[[:]] further comprising:

[[wherein]] an instruction of the plurality of bus stimuli instructions [[comprises]] comprising an instruction word having a predefined length, the instruction word having a plurality of predefined segments; [[and]]

[[wherein]] a first segment of the plurality of predefined segments [[contains]] including a type of operation[[,]] ;

a second segment of the plurality of predefined segments [[contains]] including an arbitration instruction[[,]] ;

a third segment of the plurality of predefined segments [[contains]] including address and transaction data[[,]] ; and

a fourth segment of the plurality of predefined segments [[contains]] including a data memory address.

62. (Previously Presented) The system of claim 55, further comprising an interface to a computer to receive the plurality of predefined bus stimuli instructions.

63. (Currently Amended) The system of claim 55, further comprising:

[[wherein the one or more phase generators includes]] at least one digital logic device of the phase generator coupled with the instruction memory to generate digital logic representing the plurality of bus stimuli instructions[[, and]] ;

at least one phase engine coupled between the digital logic device and the connector to translate the digital logic into the plurality of signals and to time providing the signals to the bus[[,]]; and

[[further comprising]] a response memory coupled with the at least one digital logic device to store information relating to a bus transaction phase and a response to a bus stimuli.

64. (Previously Presented) The system of claim 63:

wherein the connector comprises a connector to connect with a processor socket on a motherboard;

wherein the instruction memory comprises a static random access memory;

wherein the at least one digital logic device comprises a device selected from the group consisting of a field programmable gate array and an application specific integrated circuit; and

wherein the at least one phase engine comprises a logic level translation device.

65. (Currently Amended) The system of claim 63, further comprising:

[[wherein the at least one digital logic device comprises]] a control logic portion of the at least one digital logic device, the control logic portion to control phases

of a bus transaction including to conduct an arbitration phase and a request phase of the bus transaction[[, and]] ;

a data logic portion of the at least one digital logic device, the data logic portion to exchange data with a bus agent coupled with the bus according to the bus transaction;

[[further comprising]] a response memory coupled with the control logic portion to store information relating to a bus transaction phase and a response to a bus stimuli;

[[further comprising]] a data memory coupled with the data logic portion to store the exchanged data; and

[[wherein the at least one phase engine comprises]] a control phase engine of the at least one phase engine coupled with the control logic portion and a data phase engine of the at least one phase engine coupled with the data logic portion, the control phase engine and the data phase engine to time providing the plurality of signals on the bus.

66. (Currently Amended) A system comprising:

a connector to a bus;

an instruction memory to store a bus stimuli instruction, the instruction having a predefined length, the instruction containing a plurality of segments, the plurality of segments including at least a flow segment and a data segment;

a logic device coupled with the instruction memory to receive the bus stimuli instruction and generate digital logic based on the bus stimuli instruction, the logic device comprising a flow portion, a request portion, and a data portion, the

flow portion to receive at least the flow segment [[from the instruction memory]], and the data portion to receive at least the data segment [[from the instruction memory]], the flow portion, the request portion, and the data portion each comprising a device selected from the group consisting of a field programmable gate array and an application specific integrated circuit;

a plurality of phase engines coupled between the logic device and the connector to translate the digital logic into signals and provide the signals to the bus, the plurality of phase engines including a system phase engine, an arbitration phase engine, a request phase engine, a snoop/error phase engine, and a data phase engine, the system phase engine, the arbitration phase engine, and the request phase engine coupled with the flow portion, the snoop/error phase engine coupled with the request portion, the data phase engine coupled with the data portion;

[[further comprising]] a response memory coupled with the flow portion and the request portion to store response information; and

[[further comprising]] a data memory coupled with the data portion to store data.

67. (Previously Presented) The system of claim 66, further comprising an interface to a computer to receive the bus stimuli instruction.

68. (Previously Presented) The system of claim 66, wherein the bus stimuli instruction is based on an existing simulation stimulus software.

69. (Currently Amended) A system comprising:

a computer <u>including a DRAM memory, the computer</u> containing a <u>bus stimulus</u> file [[that is based on an existing simulation stimulus software and]] that contains a plurality of bus stimuli instructions that represent a predefined sequence of bus

transactions, [[wherein]] each bus transaction [[has]] having a plurality of transaction phases;

a processor bus;

a transaction generator containing a first connector coupled to the computer to receive the [[file]] plurality of bus stimuli instructions and containing a second connector coupled to the bus to provide a plurality of bus compatible signals to the bus, the transaction generator further containing:

an instruction memory to store the [[file]] instructions; and

[[one or more]] a phase [[generators]] generator coupled with the instruction memory to receive the plurality of bus stimuli instructions and to generate the plurality of bus compatible signals that represent the predefined sequence of bus transactions,

wherein the [[one or more]] phase generator includes [[generators include]] a logic device selected from the group consisting of a [[flow]] field programmable gate array and an application specific integrated circuit to implement the instructions as digital logic, and

wherein the [[one or more]] phase generator includes [[generators include]] a translation device coupled between the logic device and the bus to translate the digital logic to the plurality of bus compatible signals; and

a component selected from the group consisting of a processor and a chipset coupled to the bus to respond to the plurality of bus compatible signals.

70. (Previously Presented) The system of claim 69, further comprising a logic analyzer coupled with the bus to capture information associated with the response of the component to the plurality of bus compatible signals.

71. (Previously Presented) The system of claim 69, wherein the plurality of bus stimuli instructions are based on a high level language.

72. (Previously Presented) A system comprising:

an instruction memory to store a plurality of instructions representing a predefined sequence of bus transactions, wherein each transaction has multiple transaction phases; and

phase generator means for implementing the plurality of instructions on the bus as the predefined sequence of bus transactions.

73. (Previously Presented) The system of claim 72, wherein the phase generator means comprises:

logic device means for generating digital logic based on the instructions; and

phase engine means for translating the digital logic into bus logic.

74. (Currently Amended) The system of claim 72, [[contained within a second system comprising]] <u>further comprising</u> a computer coupled with the instruction memory, <u>a DRAM memory of the computer,</u> a bus coupled with the phase generator means, and a component coupled with the bus.

75. (Currently Amended) A method comprising:

coupling a component to a bus;

coupling a device comprising an instruction memory and a phase generator to the bus;

storing a plurality of instructions representing a predefined sequence of bus transactions in the instruction memory;

providing the plurality of instructions from the instruction memory to the phase generator;

[[using the phase generator to provide]] providing signals representing the predefined sequence of bus transactions to the bus with the phase generator in response to the instructions [[based on the plurality of instructions]]; and

detecting a bug of the component by determining an incorrect response of the component to the predefined sequence of bus transactions.

76. (Currently Amended) The method of claim 75, further comprising eliminating the bug [[A component designed to eliminate a bug detected by the method of claim 75, wherein the component comprises a processor]].

77. (Currently Amended) A component [[designed to eliminate]] created by eliminating a bug [[detected by the method of claim 75, wherein the component comprises a chipset]] according to the method of claim 76.

78. (Previously Presented) The method of claim 75, further comprising specifying the plurality of instructions in a high level language.

Claims 79-84 (Cancelled)

85. (Currently Amended) A method comprising:

specifying a sequence of bus transactions;

assembling the sequence into a file;

providing instructions of the file to [[a]] an instruction memory of a bus transaction generator;

providing the instructions from the instruction memory to a phase generator of the bus transaction generator;

implementing the [[predefined]] sequence of bus transactions on a bus using [[a]] the phase generator [[of the bus transaction generator]]; and

capturing a response of a component coupled with the bus to the [[predetermined]] sequence of bus transactions.

86. (Previously Presented) The method of claim 85, wherein assembling the sequence into a file comprises assembling the sequence into a binary object file.

87. (Previously Presented) The method of claim 85, wherein specifying the sequence of bus transactions comprises specifying a sequence of bus transactions in a high level language.

88. (Previously Presented) The method of claim 85, wherein capturing the response comprises capturing an incorrect response to a legal sequence of bus transactions.

89. (Previously Presented) The method of claim 85, wherein capturing the response comprises detecting a bug.

90. (New) The system of claim 55, wherein the plurality of bus stimuli instructions control the relative timing between back to back transaction phases.

91. (New) The method of claim 75, further comprising deriving the plurality of instructions from at least one selected from a bus functional model, simulation, and logic analyzer trace file.

92. (New) The method of claim 75, further comprising repeating providing signals representing the predefined sequence of bus transactions to the bus to stress the bus.

93. (New) The method of claim 85, wherein specifying the sequence of bus transactions comprises deriving the sequence from at least one selected from a bus functional model, simulation, and logic analyzer trace file.

94. (New) A method comprising:

receiving a plurality of instructions representing a predefined sequence of multiple phase bus transactions; and

providing bus stimulus signals to a bus based on the instructions.

95. (New) The method of claim 94, wherein the instructions control the relative timing between back to back transaction phases.

96. (New) The method of claim 94, wherein the instructions comprise user specified instructions and are based on a high level language.